Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): A method for fabricating a routing layout design, the method comprising:

(a) forming a plurality of metal traces on a first routing layer and a second routing layer, comprising:

positioning a plurality of first conducting wires and a plurality of second conducting wires on a plurality of horizontal tracks and a plurality of vertical tracks of the first routing layer respectively; and

positioning a plurality of third conducting wires and a plurality of fourth conducting wires on a plurality of horizontal tracks and a plurality of vertical tracks of the second routing layer respectively, the third conducting wire on a k^{th} horizontal track of the second routing layer vertically overlapping the first conducting wire on the k^{th} horizontal track of the first routing layer; and

(b) positioning a plurality of vias within a via layer disposed between the first and second routing layers for connecting the metal traces on the first and second routing layers according to a first current route defined by a predetermined circuit layout design used for connecting a first node and a second node so as to establish a second current route equivalent to the first current route.

2 (cancelled).

3 (currently amended): The method of ~~claim 2~~ claim 1, wherein the step (b) comprises:

positioning one of the vias within the via layer for electrically

connecting the first conducting wire on the k^{th} horizontal track of the first routing layer and the third conducting wire on the k^{th} horizontal track of the second routing layer when the first node and the second node are electrically connected to the first conducting wire on the k^{th} horizontal track of the first routing layer and the third conducting wire on the k^{th} horizontal track of the second routing layer respectively.

4-13 (cancelled).

14 (original): The method of claim 1, wherein the metal traces on the first routing layer and the corresponding metal traces on the second routing layer have substantially the same lengths.

15 (original): The method of claim 1 being applied to a multi-layer circuit board.

16 (original): The method of claim 1 being applied to a semiconductor device.

17-20 (cancelled).

21 (new): A method for fabricating a routing layout design, the method comprising:

(a) forming a plurality of metal traces on a first routing layer and a second routing layer, comprising:

positioning a plurality of first conducting wires and a plurality of second conducting wires on a plurality of horizontal tracks and a plurality of vertical tracks of the first routing layer respectively; and

positioning a plurality of third conducting wires and a plurality of fourth

conducting wires on a plurality of horizontal tracks and a plurality of vertical tracks of the second routing layer respectively, the third conducting wire on an m^{th} horizontal track of the second routing layer partially overlapping the second conducting wire on an n^{th} vertical track of the first routing layer; and

(b) positioning a plurality of vias within a via layer disposed between the first and second routing layers for connecting the metal traces on the first and second routing layers according to a first current route defined by a predetermined circuit layout design used for connecting a first node and a second node so as to establish a second current route equivalent to the first current route.

22 (new): The method of claim 21, wherein the step (b) comprises:

positioning one of the vias within the via layer for electrically connecting the second conducting wire on the n^{th} vertical track of the first routing layer and the third conducting wire on the m^{th} horizontal track of the second routing layer when the first node is electrically connected to the second conducting wire on the n^{th} vertical track of the first routing layer and the second node is electrically connected to the third conducting wire on the m^{th} horizontal track of the second routing layer.

23 (new): The method of claim 21, wherein the third conducting wire on the m^{th} horizontal track of the second routing layer partially overlaps the first conducting wire on the m^{th} horizontal track of the first routing layer, and the first conducting wire on the m^{th} horizontal track of the first routing layer partially overlaps the fourth conducting wire on the $n^{th}+1$ vertical track of the second routing layer.

24 (new): The method of claim 21, wherein the second conducting wire on the n^{th} vertical track of the first routing layer partially overlaps the fourth conducting wire on the n^{th} vertical track of the second routing layer, and the first conducting wire on the $m^{th}+1$ horizontal track of the first routing layer partially overlaps the fourth conducting wire on the n^{th} vertical track of the second routing layer.

25 (new): A method for fabricating a routing layout design, the method comprising:

(a) forming a plurality of metal traces on a first routing layer and a second routing layer, comprising:

positioning a plurality of first conducting wires and a plurality of second conducting wires on a plurality of horizontal tracks and on a plurality of vertical tracks of the first routing layer respectively; and

positioning a plurality of third conducting wires and a plurality of fourth conducting wires on a plurality of horizontal tracks and on a plurality of vertical tracks of the second routing layer respectively, the fourth conducting wire on an r^{th} vertical track of the second routing layer partially overlapping the second conducting wire on the r^{th} vertical track of the first routing layer; and

(b) positioning a plurality of vias within a via layer disposed between the first and second routing layers for connecting the metal traces on the first and second routing layers according to a first current route defined by a predetermined circuit layout design used for connecting a first node and a second node so as to establish a second current route equivalent to the first current route.

26 (new): The method of claim 25, wherein the step (b) comprises:

positioning one of the vias within the via layer for electrically connecting the second conducting wire on the r^{th} vertical track of the first routing layer and the fourth conducting wire on the r^{th} vertical track of the second routing layer when the first node is electrically connected to the second conducting wire on the r^{th} vertical track of the first routing layer and the second node is electrically connected to the fourth conducting wire on the r^{th} vertical track of the second routing layer.

27 (new): A method for fabricating a routing layout design, the method comprising:

(a) forming a plurality of metal traces on a first routing layer and a second routing layer, comprising:

positioning a plurality of first conducting wires and a plurality of second conducting wires on a plurality of horizontal tracks and on a plurality of vertical tracks of the first routing layer respectively; and

positioning a plurality of third conducting wires and a plurality of fourth conducting wires on a plurality of horizontal tracks and on a plurality of vertical tracks of the second routing layer respectively, the fourth conducting wire on an s^{th} vertical track of the second routing layer partially overlapping the first conducting wire on a t^{th} horizontal track of the first routing layer; and

(b) positioning a plurality of vias within a via layer disposed between the first and second routing layers for connecting the metal traces on the first and second routing layers according to a first current route defined by a predetermined circuit layout design used for connecting a first node and a second node so as to establish a second current route equivalent to the first current route.

28 (new): The method of claim 27, wherein the step (b) comprises:

positioning one of the vias within the via layer for electrically connecting the first conducting wire on the t^{th} horizontal track of the first routing layer and the fourth conducting wire on the s^{th} vertical track of the second routing layer when the first node is electrically connected to the first conducting wire on the t^{th} horizontal track of the first routing layer and the second node is electrically connected to the fourth conducting wire on the s^{th} vertical track of the second routing layer.

29 (new): The method of claim 27, wherein the first conducting wire on the t^{th} horizontal track of the first routing layer partially overlaps the third conducting wire on the t^{th} horizontal track of the second routing layer, and the third conducting wire on the t^{th} horizontal track of the second routing layer partially overlaps the second conducting wire on the $s^{th}+1$ vertical track of the first routing layer.

30 (new): The method of claim 27, wherein the second conducting wire on the s^{th} vertical track of the second routing layer partially overlaps the second conducting wire on the s^{th} vertical track of the first routing layer, and the second conducting wire on the s^{th} vertical track of the first routing layer partially overlaps the third conducting wire on the $t^{th}+1$ horizontal track of the first routing layer.